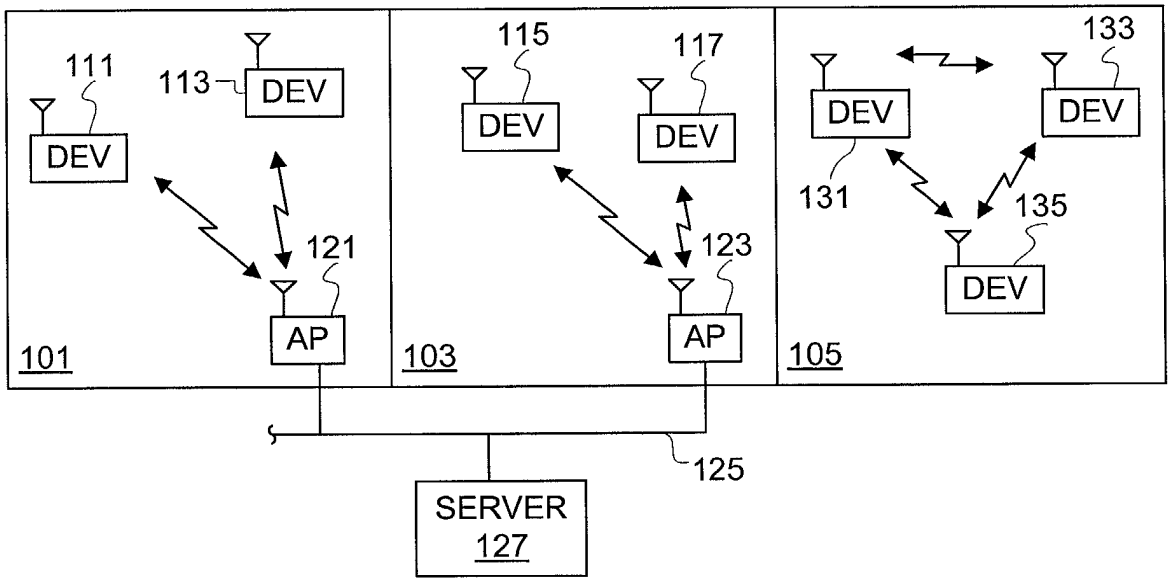

111
113
DEV
DEV
121
AP
101
115
117
DEV
DEV
123
AP
103
133
DEV
DEV
131
135
DEV
105
125
SERVER
127

FIG. 1

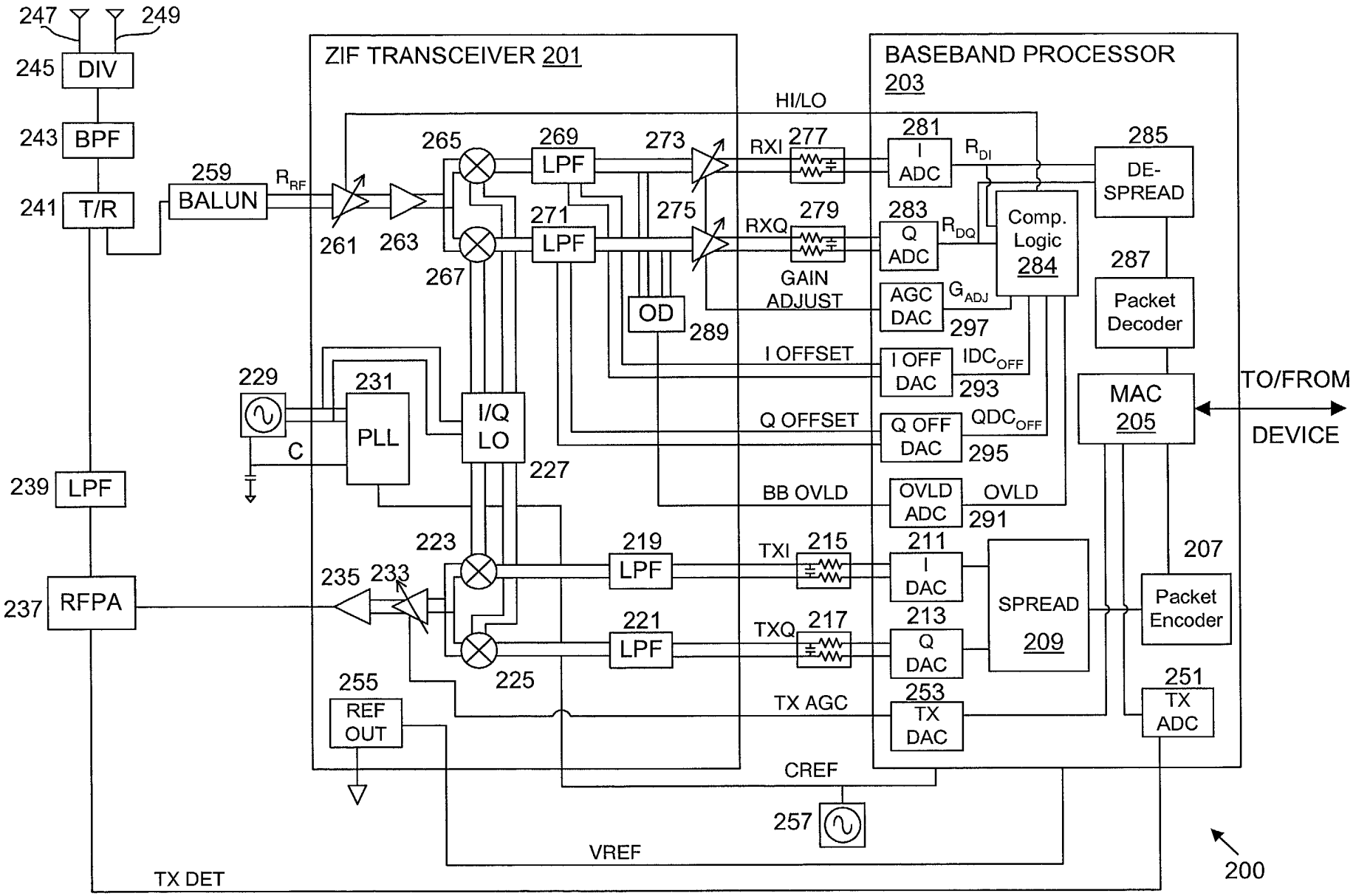

247
249
245
DIV
243
BPF
241
T/R
259
BALUN
R_{RF}
261
263
ZIF TRANSCEIVER 201
BASEBAND PROCESSOR 203
HI/LO
265
269
LPF
273
RXI
277
281
I ADC
R_{DI}
285
DE-SPREAD
271
LPF
275
RXQ
279
283
Q ADC
R_{DQ}
Comp. Logic 284
287
Packet Decoder
267
GAIN ADJUST
AGC DAC
G_{ADJ}
297
OD
289
I OFFSET
I OFF DAC
IDC_{OFF}
293
229
231
PLL
I/Q LO
227
C
Q OFFSET
Q OFF DAC
QDC_{OFF}
295
MAC 205
TO/FROM DEVICE
239
LPF
BB OVLD
OVLD ADC
OVLD
291
223
219
LPF
TXI
215
211
I DAC
207
235
233
237
RFPA
SPREAD 209
Packet Encoder
221
LPF
TXQ
217
213
Q DAC
225
255
REF OUT
TX AGC
253
TX DAC
251
TX ADC
CREF
257
VREF
TX DET
200

FIG. 2

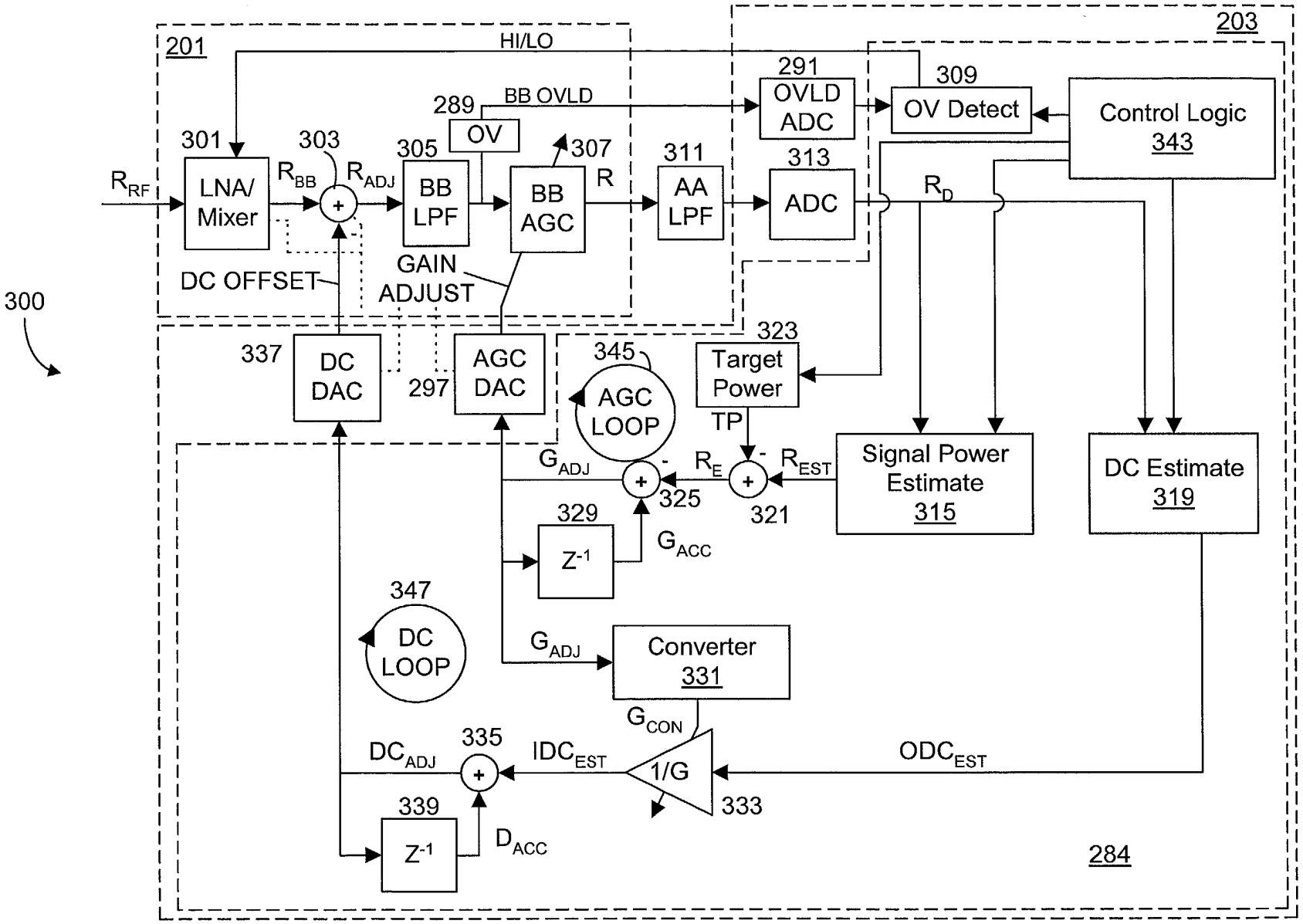

300
201
203
HI/LO
289
BB OVLD
OV
291
OVLD ADC
309
OV Detect
Control Logic
343
301
303
305
307
311
313
R_{RF}
LNA/ Mixer
R_{BB}
R_{ADJ}
BB LPF
BB AGC
R
AA LPF
ADC
R_D
DC OFFSET
GAIN ADJUST
337
DC DAC
297
AGC DAC
345
AGC LOOP
323
Target Power
TP
G_{ADJ}
R_E
R_{EST}
325
321
Signal Power Estimate
315
DC Estimate
319
329
Z^{-1}
G_{ACC}
347
DC LOOP
G_{ADJ}
Converter
331
G_{CON}
335
DC_{ADJ}
IDC_{EST}
1/G
ODC_{EST}
333
339
Z^{-1}
D_{ACC}
284

FIG. 3

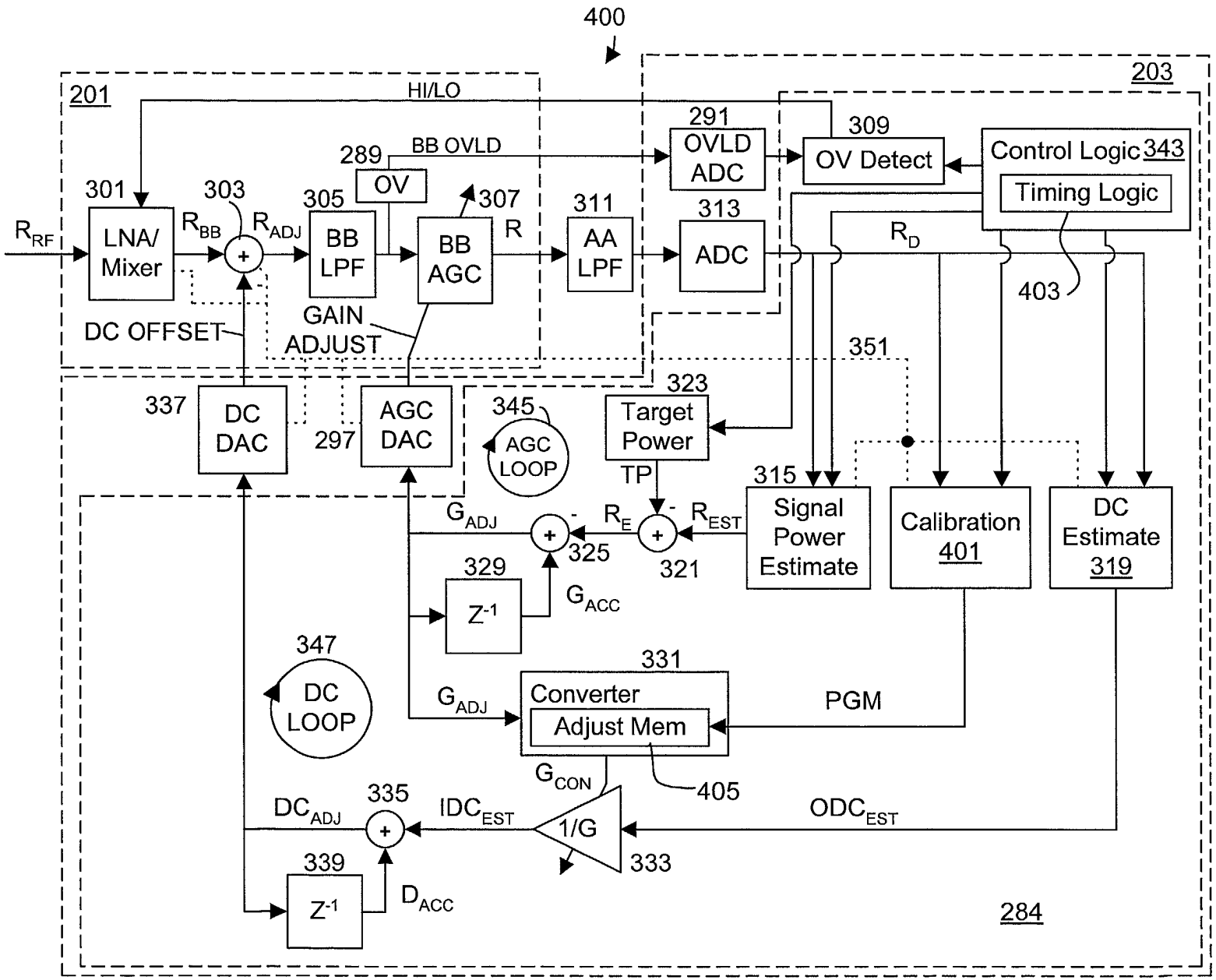


FIG. 4

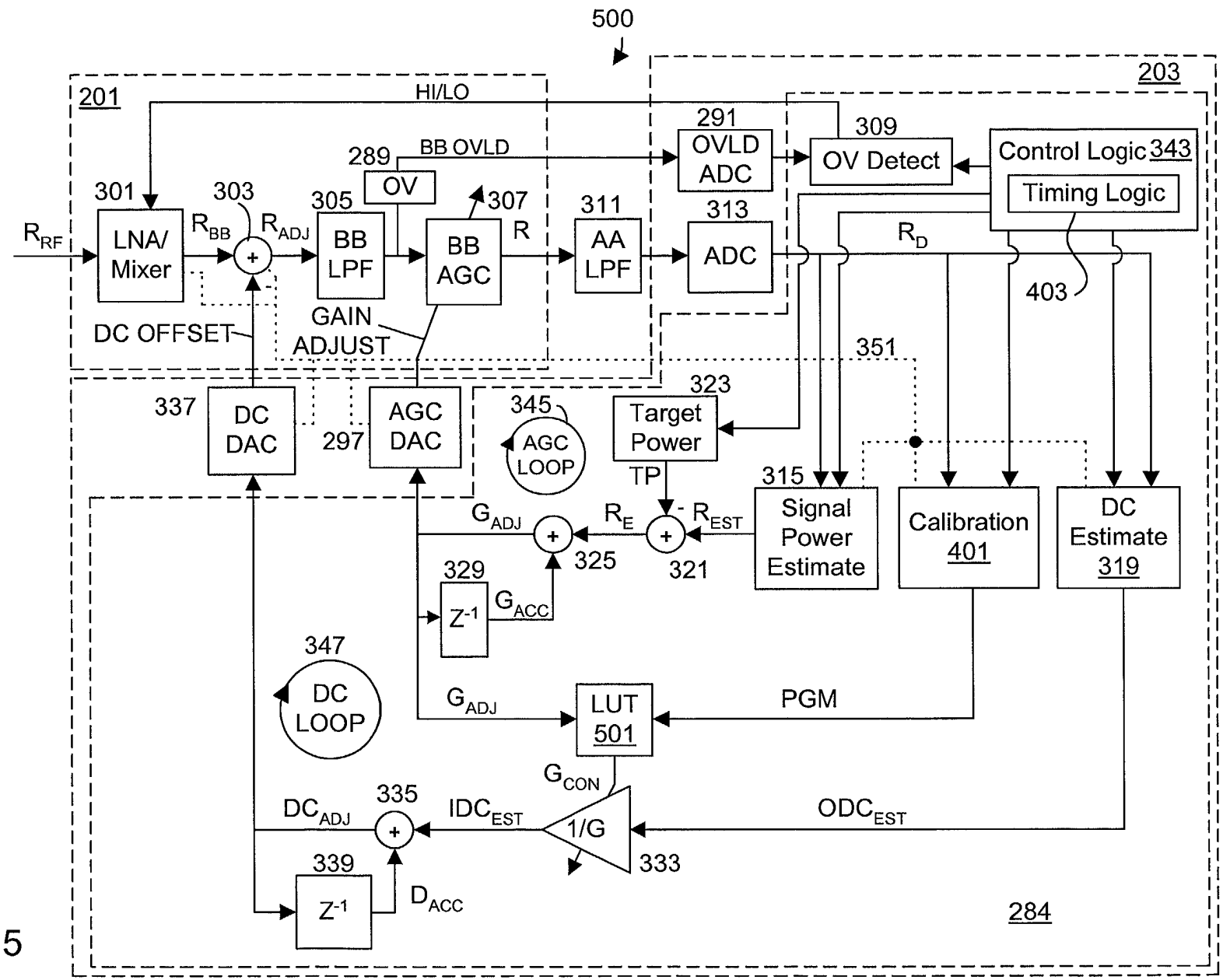


FIG. 5

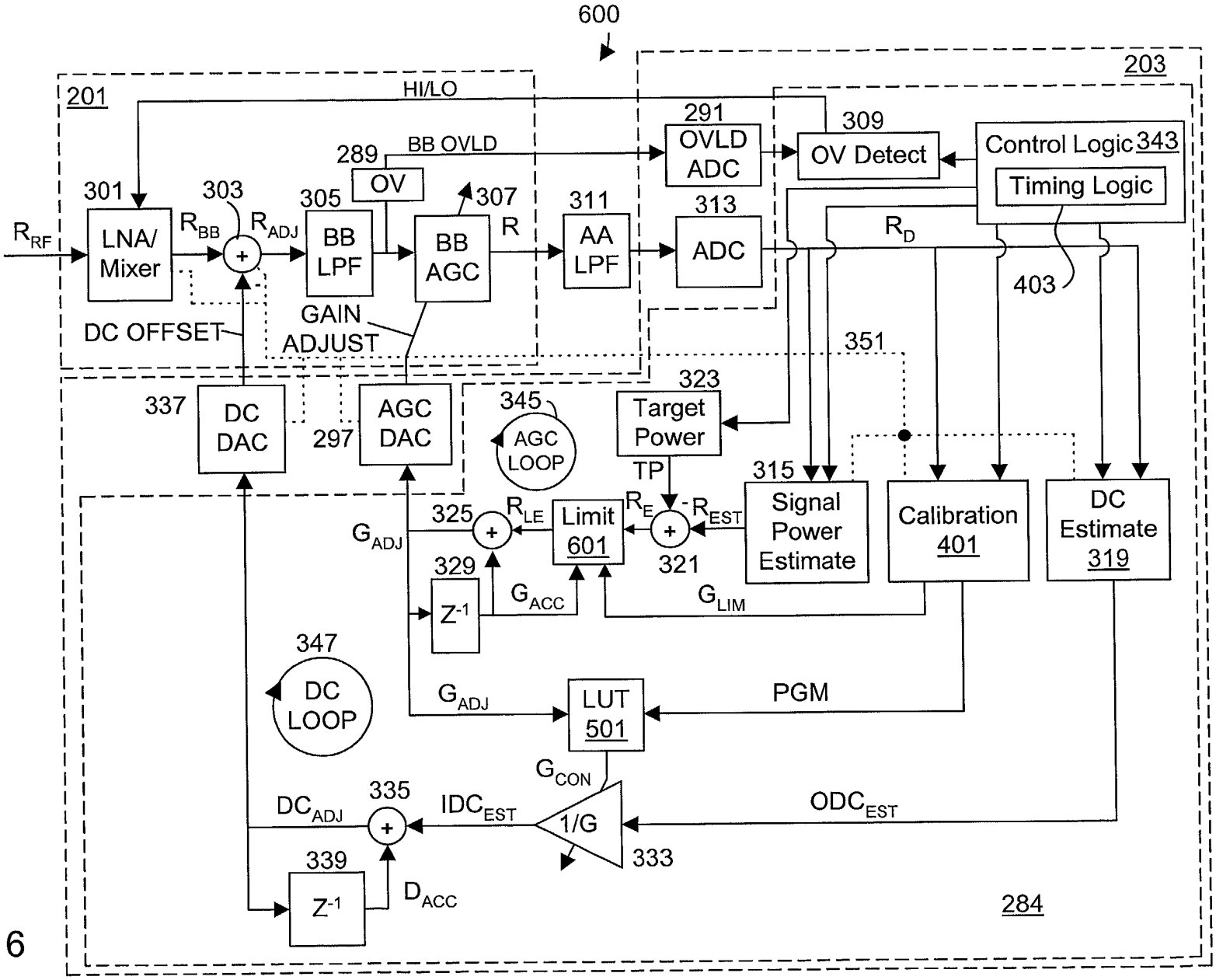


FIG. 6

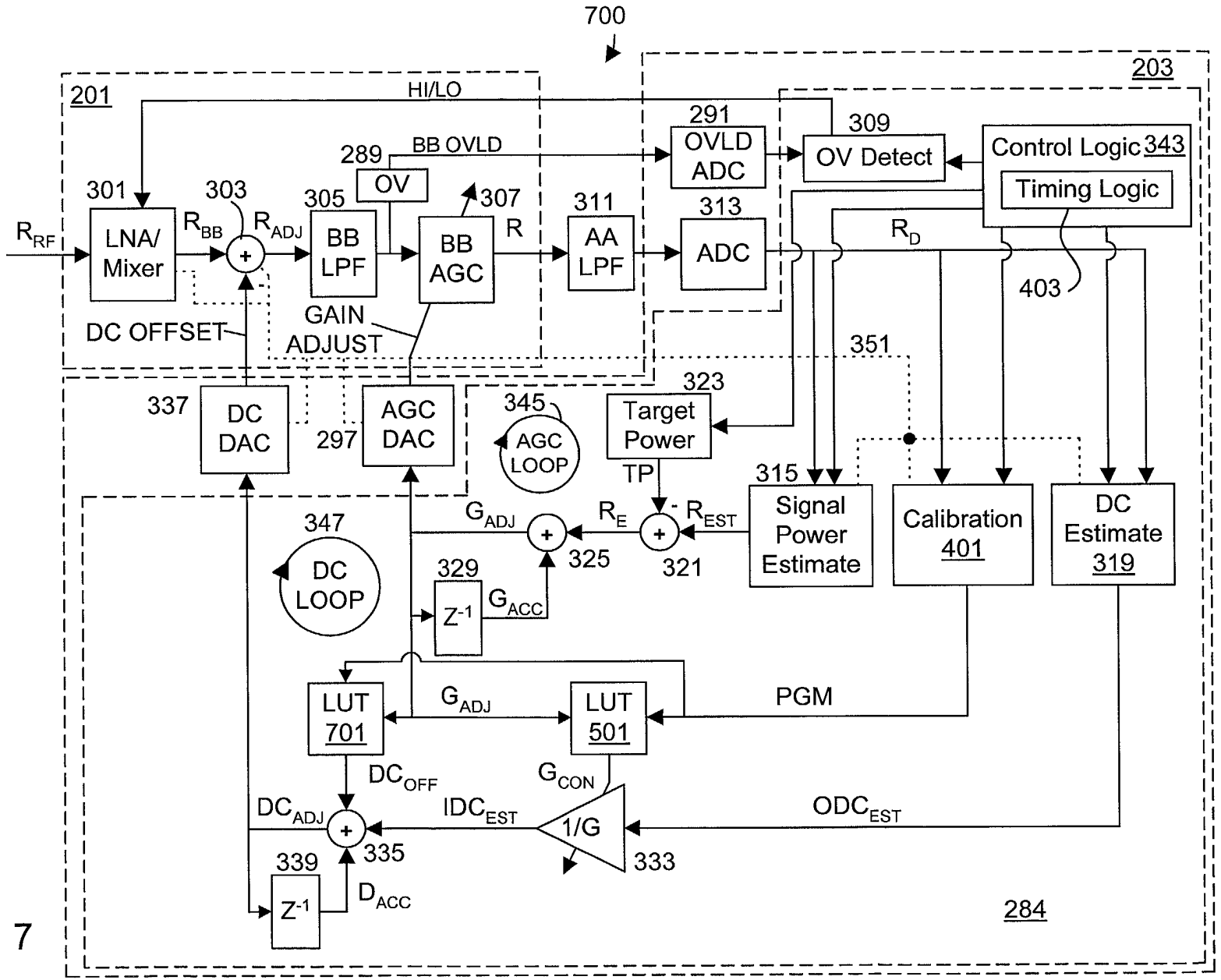
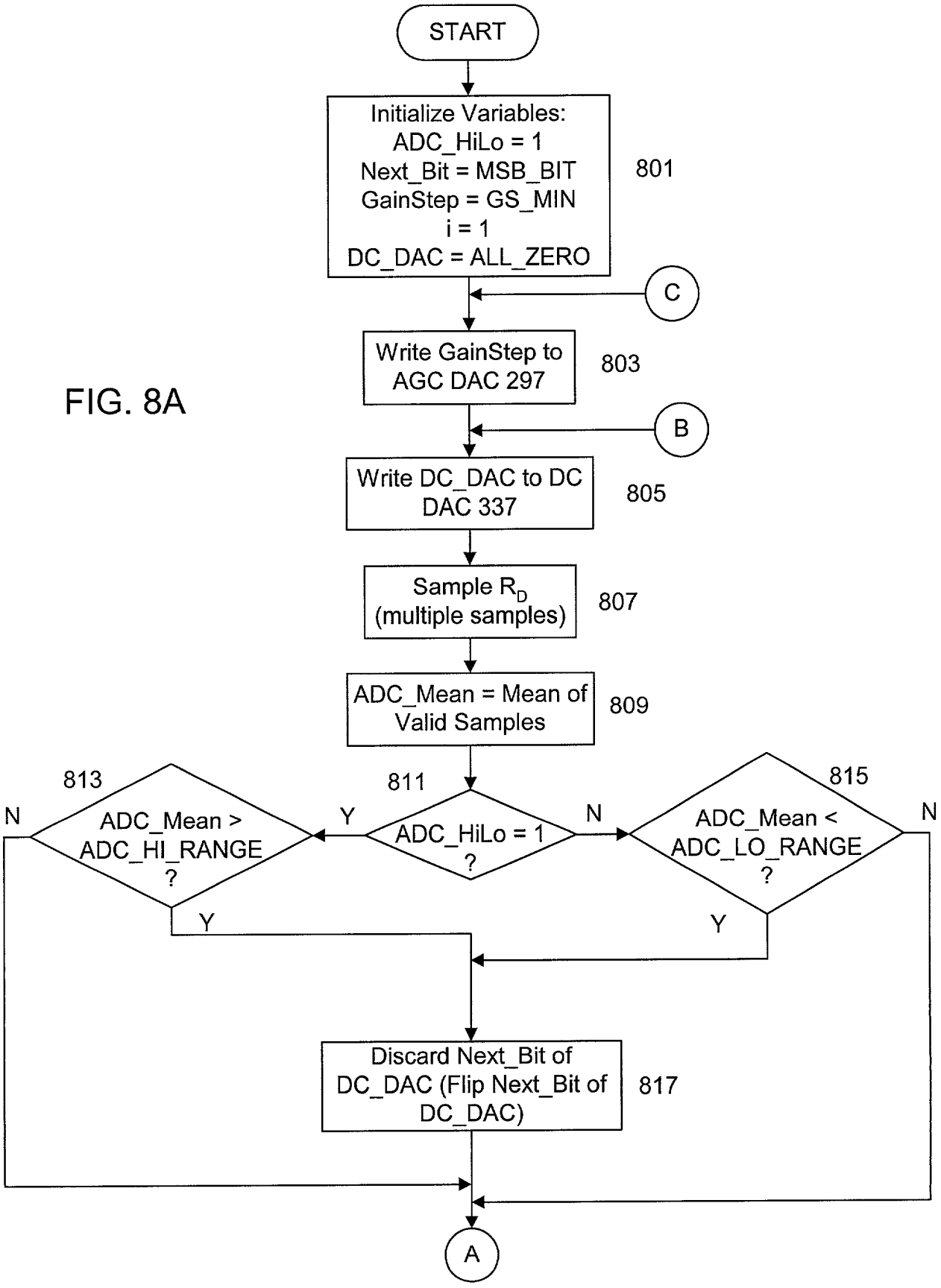


FIG. 7

FIG. 8A


START
Initialize Variables:
ADC_HiLo = 1
Next_Bit = MSB_BIT
GainStep = GS_MIN
i = 1
DC_DAC = ALL_ZERO
801
C
Write GainStep to AGC DAC 297
803
B
Write DC_DAC to DC DAC 337
805
Sample R_D (multiple samples)
807
ADC_Mean = Mean of Valid Samples
809
811
ADC_HiLo = 1 ?
Y
N
813
ADC_Mean > ADC_HI_RANGE ?
N
Y
815
ADC_Mean < ADC_LO_RANGE ?
N
Y
Discard Next_Bit of DC_DAC (Flip Next_Bit of DC_DAC)
817
A

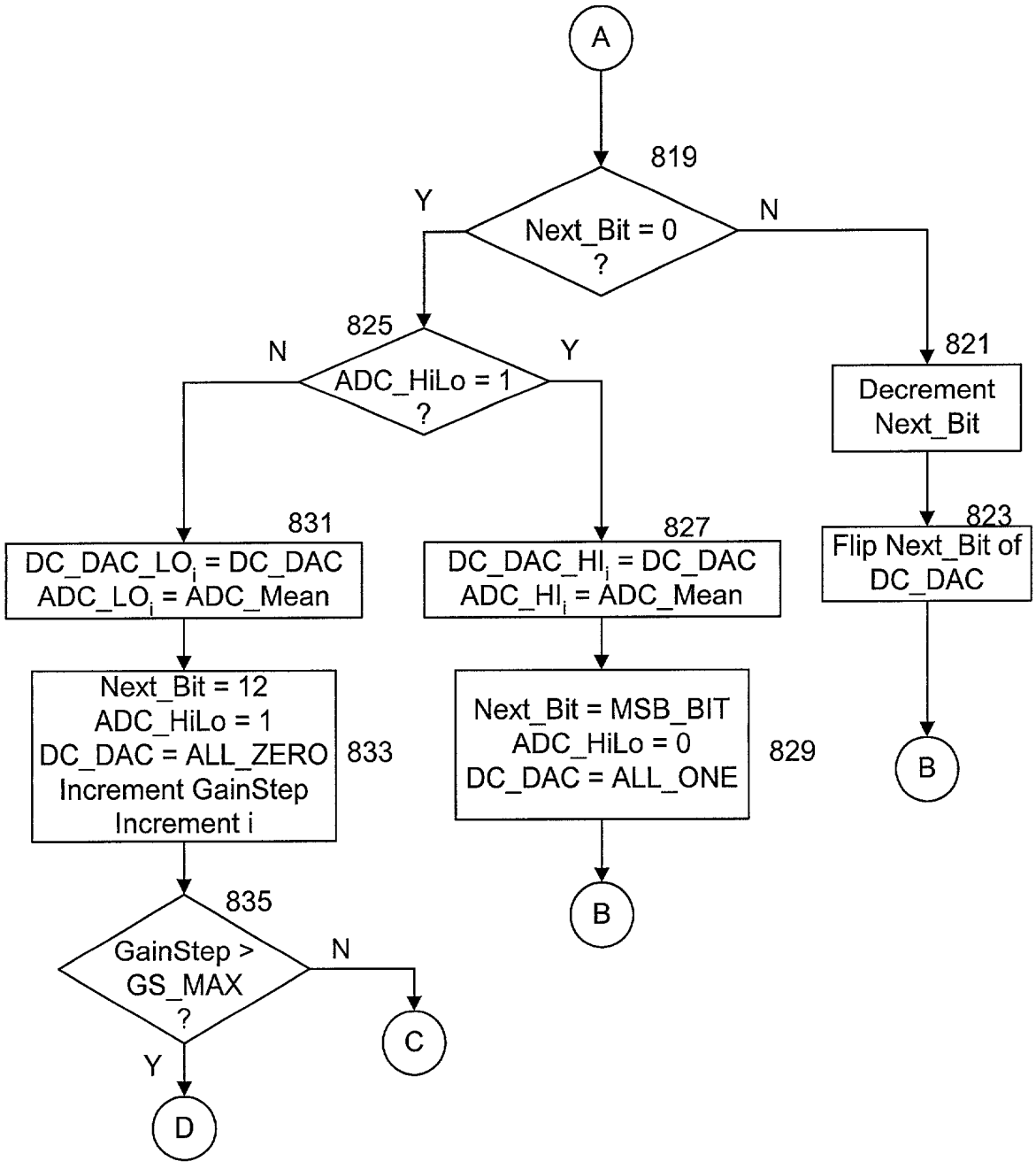

A
819
Next_Bit = 0 ?
Y
N
825
ADC_HiLo = 1 ?
N
Y
821
Decrement Next_Bit
823
Flip Next_Bit of DC_DAC
B
831
DC_DAC_LO$_i$ = DC_DAC
ADC_LO$_i$ = ADC_Mean
827
DC_DAC_HI$_i$ = DC_DAC
ADC_HI$_i$ = ADC_Mean
Next_Bit = 12
ADC_HiLo = 1
DC_DAC = ALL_ZERO
Increment GainStep
Increment i
833
Next_Bit = MSB_BIT
ADC_HiLo = 0
DC_DAC = ALL_ONE
829
B
835
GainStep > GS_MAX ?
N
C
Y
D

FIG. 8B

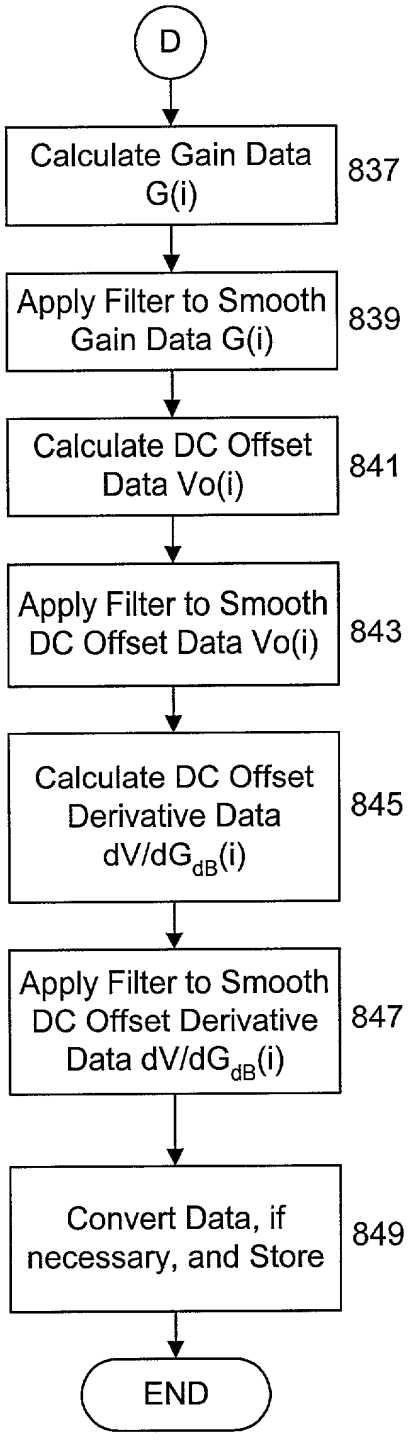

D
Calculate Gain Data G(i)
837
Apply Filter to Smooth Gain Data G(i)
839
Calculate DC Offset Data Vo(i)
841
Apply Filter to Smooth DC Offset Data Vo(i)
843
Calculate DC Offset Derivative Data dV/dG_dB(i)
845
Apply Filter to Smooth DC Offset Derivative Data dV/dG_dB(i)
847
Convert Data, if necessary, and Store
849
END

FIG. 8C

AGC Onset Timeline

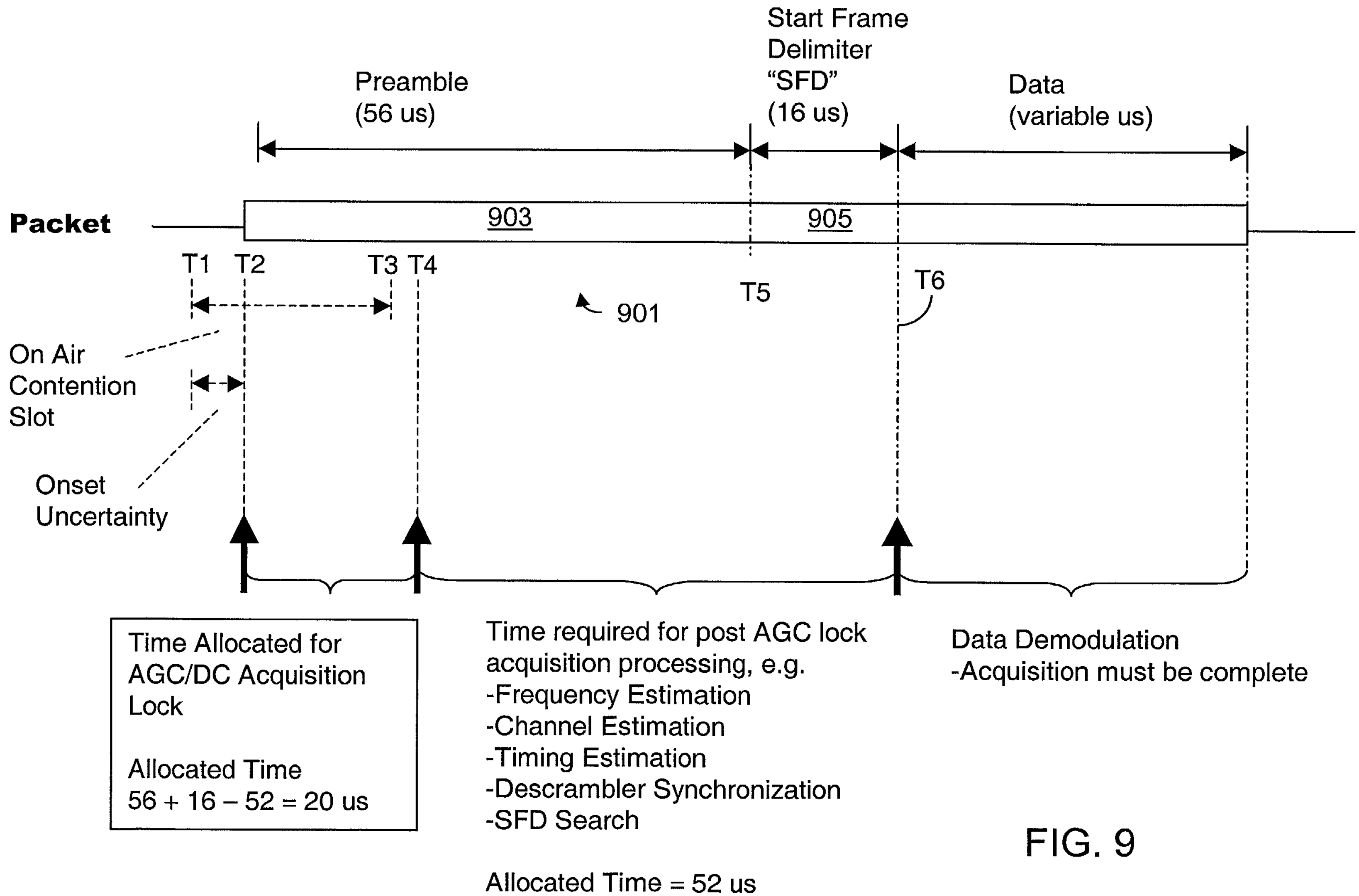


FIG. 9

ACK Priority Acquisition Timeline

Packet transmission and AGC/DC turnaround for successful packet reception.

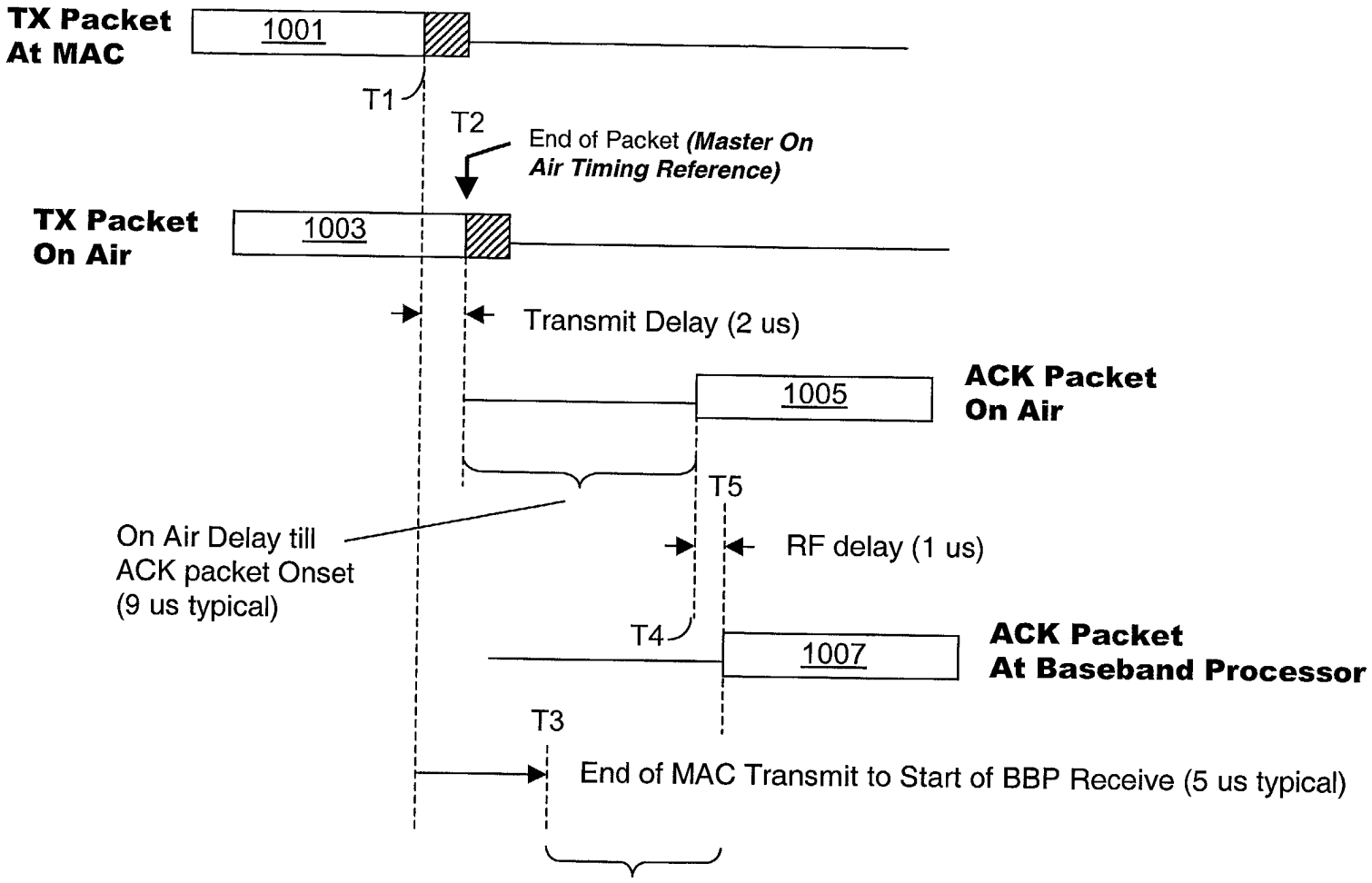


FIG. 10

Time Budgeted for AGC/DC Pre ACK Onset Restoration Attempt
2 + 9 + 1 – 5 = 7 us

CCA Priority Acquisition Timeline

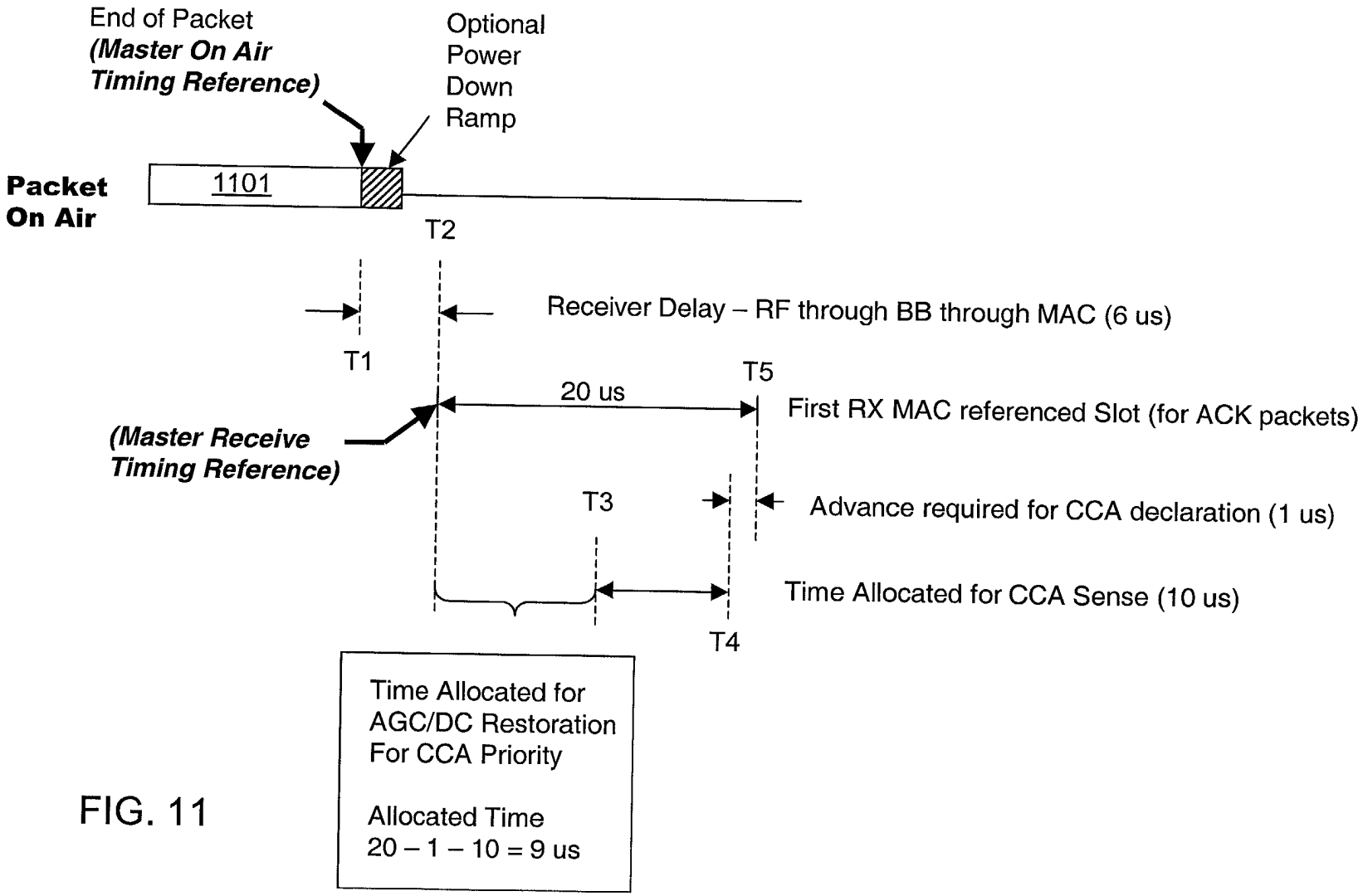


FIG. 11